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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/811,456	03/20/01	ISODA M	108075-00056

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EXAMINER	
NGUYEN,L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/19/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/811,456	ISODA, MASAHITO	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2001* .

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-15* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/479,927* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to because the black boxes in Figure 6 have not been provided with text labels. Correction is required.

The drawings are also objected to because the two switches in Figure 6 have not been provided with a respective reference numeral. Correction is required.

The drawings are also objected to because circuit 1 in Figure 6 is incorrect or confusing. The detail of transfer circuit 4 is shown in Figure 2 in which the transfer circuit receives an input signal IN and output a signal that has the same logical level as the input signal IN. However, Figure 6 shows that the transfer circuit 4 is a tri-state inverter, which the output does not have the same logical level as the input signal IN.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12 and 13 are indefinite because the recitation "small" in claim 12 and "full" in claim 13 are indefinite relative terms, i.e., it is not clear how small or large the amplitudes of the first and the second input signals must be to meet these claims. Also, the recitation "when the first and second input signals ... amplitude" on the last two lines of these claims appears to cause these claims to be misdescriptive because it is seen that the control circuit (17, Figure 5) is

independent with the first and second input signals (IN, IN/) of the input buffer circuit (Figure 5). Therefore, the amplitude of the first and second input signals does not affect when the control circuit disable/or enable the differential amplifier, the first or the second tri-state inverter circuit.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Roe et al. (USP 5,929,655).

With respect to claim 11, Figure 3 of the Roe et al. reference disclose an input buffer circuit which includes: a differential amplifier circuit (210) for receiving first and second input signals (140, 146) and generating an amplifier signal (output of 210) corresponding to a voltage difference between the first and second input signals; a first tri-state inverter circuit (208) for receiving the amplified signal from the differential amplifier circuit; a second tri-state inverter circuit (202) for receiving the first input signal (140); and a control circuit (214), connected to the differential amplifier circuit (210) and the first (208) and the second (202) tri-state inverter circuits, for selectively enabling the differential amplifier circuit and the first and second tri-state inverter circuits in accordance with a control signal (DIFF_EN, OUTA_EN, OUTB_EN).

Insofar as understood in claims 12 and 13, it is seen in Figure 3 of the Roe et al. reference that the control circuit enables the differential amplifier circuit and the first tri-state inverter circuit and disables the second tri-state inverter circuit; and vice versa.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roe et al. (USP 5,929,655) in view of Oldham (USP 5,563,835).

With respect to claim 14, Figure 3 of the Roe et al. reference discloses an input buffer circuit which teaches all limitations of this claim as discussed in the 102 rejections except for that the input buffer includes a driver circuit, connected to the first and second tri-state inverter circuits, for receiving an output signal from the enabled one of the first and second tri-state inverter circuits. However, it is seen that the output signals (OUT_A and OUT_B) in Figure 3 of the Roe reference are usable to drive any circuitry; and Figure 2 of the Oldham reference discloses a driver circuit (111, 112) connected to a differential output signal (output of 110 and 120) to convert differential output to single output to drive another downstream circuitry. Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the input buffer in Figure 3 of the Roe et al. reference by adding a driver circuit (111, 112) as in Figure 7 of the Aoki reference to the differential output signals (OUT_A and OUT_B) in Figure 3 of the Roe et al. reference to convert the differential output signal to a single output signal to drive another downstream circuitry. It is clear that such modification meets the limitations of claim 14.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roe et al. (USP 5,929,655) in view of D'Souza (USP 5,811,992).

With respect to claim 15, Figure 3 of the Roe et al. reference discloses an input buffer circuit which teaches all limitations of this claim except for the detail of the first and second tri-state inverters wherein each includes an inverter, a PMOS transistor and an NMOS transistor, which the recited connected set forth in claim 15. However, Figure 2 of the D'Souza reference discloses a tri-state inverter circuit which includes an inverter (the PMOS and NMOS connected to DIN), a PMOS transistor (connected to CLKB), and an NMOS transistor (connected to CLK) with the recited connection set forth in claim 15. Therefore, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify the input buffer in Figure 3 of the Roe et al. reference by using a specific tri-state inverter circuit such as in Figure 2 of the D'Souza reference for broad tri-state inverter circuits because it functions equivalent and it is well known that this specific tri-state inverter's structure offers less delay than other tri-state inverter's structures.

Allowable Subject Matter

9. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 16 would be allowed because none of the prior art of record discloses or suggests an input buffer circuit which includes all the limitations of this claim. In particular, the prior art of record fails to disclose or suggest that the control circuit (17, Figure 5) generates first (S) and second (S/) control signals which are complementary to each other; wherein the PMOS (Tp9,

Figure 5) of the first tri-state inverter (13, Figure 5) and the NMOS (Tn9, Figure5) of the second tri-sate inverter (14, Figure5) are controlled by the first control signal (S); and wherein the NMOS (Tn8, Figure 5) of the first tri-state inverter (13, Figure 5) and the PMOS (Tp10, Figure5) of the second tri-sate inverter (14, Figure5) are controlled by the second control signal (S/).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Long Nguyen whose telephone number is (703) 308-6063. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for this group is (703) 308-7722.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

October 16, 2001

LN

Long Nguyen
Art Unit: 2816

Terry D. Cunningham
Primary Examiner